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(71) Applicant: **Omnivision Technologies Inc.**
Sunnyvale, California 94085 (US)

(72) Inventor: **Dai, Tiejun**
Santa Clara, California 95050 (US)

(74) Representative: **Hackney, Nigel John et al**
Mewburn Ellis,
York House,
23 Kingsway
London WC2B 6HP (GB)

(54) Zero DC current readout circuit for cmos image sensor

(57) A method of reading out a light signal from a pixel is disclosed. The method comprises first charging a capacitor to a predetermined voltage during a precharge stage. Next, during a readout stage, discharging the capacitor for a predetermined length of time through a pixel output transistor. The pixel output transistor is modulated by the light signal by applying the light signal to the gate of the pixel output transistor. Finally, the output signal is determined to be the voltage held by the capacitor.

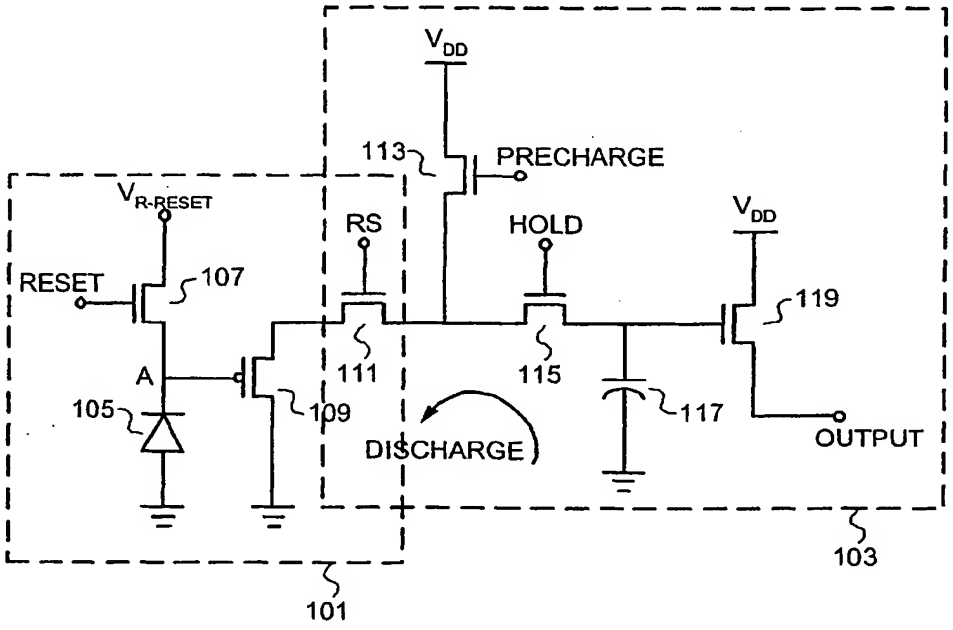

FIGURE 1

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Description

[0001] The present invention relates to CMOS image sensors used in scanners, and more particularly, to a readout circuit in the CMOS image sensor that draws no DC current during readout.

[0002] Scanners are commonly used in connection with a personal computer (PC) to digitize a document. The document may be a textual document or other type of document, such as a photograph. One of the important components of a scanner is the imaging device. In many modern scanners, the imaging device is a CCD image sensor. Recently, CMOS image sensors have made significant inroads into applications previously dominated by CCD image sensors. This is due in part to the lower cost and lower power consumption of CMOS image sensors. These advantages are particularly important in PC camera applications, security applications, cell phone applications, and the like.

[0003] Depending upon the particular application, CMOS image sensors come in a variety of array sizes. High-resolution image sensors with over one million pixels are used in digital still cameras, while lower resolution CIF, VGA, or SVGA formats are used for security camera or PC camera applications. In many applications, the pixel array size is on the order of 352-1280 pixels per row with 288-1024 pixels per column.

[0004] For scanner applications, the pixel array has significantly different dimensions. Typically, approximately 10,000 pixels are in each row. Specifically, most scanners are manufactured to scan documents 8.5 inches wide. At a resolution of 1200 dots per inch (dpi), this requires a little over 10,000 pixels. Further, a black and white scanner will only require a single row of pixels. However, for a color scanner, three rows of 10,000 pixels are required, one row for the color red, one row for the color green, and one row for the color blue.

[0005] During readout of the signals from each pixel in the array, there is typically a current associated with the readout process. If a large number of pixels must be read out simultaneously, then a large current is required. The large current required will also cause a voltage drop in the power supply line and also affect the ground line of the image sensor. This in turn will cause non-uniformity and decrease in the signal range of the image sensor.

[0006] While this is an issue for many image sensors, the problem is complicated by the need to read out over 30,000 pixels simultaneously for a color image sensor used in a scanner. Moreover, because of the large number of pixels in a row, the actual dimension of the pixel array is on the order of 2 centimeters. Because of this, the metal lines used as power and ground are unusually long compared to image sensors used in other applications. For this additional reason, the voltage drop in the power and ground lines is problematical.

[0007] In a first aspect the present invention provides a readout circuit according to claim 1.

Brief Description of the Drawings

[0008] The foregoing aspects and many of the attendant advantages of the invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic diagram of a readout circuit formed in accordance with the present invention.

Figure 2 is a schematic diagram of a readout circuit formed in accordance with an alternative embodiment of the present invention.

Figure 3 is a schematic diagram of a readout circuit formed in accordance with another alternative embodiment of the present invention.

Figure 4 is a schematic diagram of a readout circuit formed in accordance with yet another alternative embodiment of the present invention.

Figure 5 is a schematic diagram of a readout circuit formed in accordance with yet another alternative embodiment of the present invention.

Detailed Description of the Preferred Embodiment

[0009] In the following description, numerous specific details are provided, such as the identification of various system components, to provide a thorough understanding of embodiments of the invention. One skilled in the art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In still other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of various embodiments of the invention.

[0010] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0011] As noted above, a CMOS image sensor includes an array of pixels formed into columns and rows. For a color scanner application, the array consists of three rows of pixels, one for each primary color. Each of these pixels must be read out in some manner. Typically, each column of pixels has associated therewith a readout circuit, which is the subject of the present invention. In the description below, a single pixel is described in connection with a readout circuit. It can be appreciated that multiple readout circuits would be required for the

full image sensor.

[0012] Turning to Figure 1, an active pixel 101 is shown connected to a readout circuit 103. The active pixel 101 includes a photodiode 105, a reset transistor 107, pixel output transistor 109, and row select transistor 111. The readout circuit 103 includes a precharge transistor 113, a hold transistor 115, a capacitor 117, and an amplifying output transistor 119. Because the row select transistor 111, in some interpretations, may not be explicitly considered part of the pixel 101, the row select transistor 111, alternatively, may be considered part of the readout circuit 103. Similarly, the pixel output transistor 109 may also be considered as a part of the readout circuit 103.

[0013] The photodiode is connected between ground and the source of reset transistor 107 at a node A. The drain of reset transistor 107 is connected to a voltage rail set at a value (V_{R_reset}). V_{R_reset} is a reference voltage, which could be in one embodiment V_{DD}, or a value lower than V_{DD}. The gate of the reset transistor 107 is controlled by a reset signal line. The reset transistor 107 operates as a switch that is controlled by the reset signal line.

[0014] Further, the source of the reset transistor 107 (corresponding to the "output" of the photodiode 105) is connected to the gate of the pixel output transistor 109. In this manner, the pixel output transistor 109 is designed such that the voltage output by the photodiode 105 will cause the pixel output transistor 109 to operate in the linear region. As will be seen below, this will modulate the magnitude of a signal to be output. In one embodiment, the pixel output transistor 109 is a PMOS, however, as will be seen below in other embodiments, an NMOS may also be used.

[0015] The pixel output transistor 109 is connected between ground and the source or drain of row select transistor 111. The gate of the row select transistor 111 is connected to a row select (RS) signal line. The row select transistor 111 operates as a switch that is controlled by the row select signal line.

[0016] The source or drain of the row select transistor 111 is connected to the source or drain of the hold transistor 115. The gate of the hold transistor 115 is connected to a hold signal line. The hold transistor 115 operates as a switch that is controlled by the hold signal line.

[0017] Also connected to the source or drain of the row select transistor 111 is the source of the precharge transistor 113. The gate of the precharge transistor 113 is connected to a precharge signal line. The precharge transistor 113 operates as a switch that is controlled by the precharge signal line.

[0018] The drain of the hold transistor 115 is connected to one terminal of the capacitor 117. The other terminal of the capacitor 117 is connected to ground. Further, the drain of the hold transistor 115 is connected to the gate of the output transistor 119. In this conventional amplification configuration, the amplifying output transistor 119 serves as an amplification element.

[0019] In this embodiment, the readout circuit 103 operates in two stages, a precharge stage and a readout stage. In the precharge stage, the row select signal is low, causing the row select transistor 111 to be off. The precharge signal and hold signal is high, causing the precharge transistor 113 and hold transistor 115 to be on. This causes the voltage V_{DD} to be placed on capacitor 117, thereby charging the capacitor 117. After the capacitor 117 has been charged, the precharge signal and hold signal is then put to low, causing the precharge transistor 113 and hold transistor 115 to be off.

[0020] During the readout stage, the row select signal and the hold signal is high, turning on the both of these transistors 111 and 115. This will cause the capacitor 117 to discharge via a current flowing through the pixel output transistor 109. The discharge current decreases rapidly with time. After a predetermined and consistent amount of time, the row select signal and the hold signal is then put to low, turning off the both of these transistors 111 and 115, and ending the discharge process.

[0021] The rate at which the capacitor 117 is discharged is controlled by the signal on the gate of pixel output transistor 109. If a high signal is output by the photodiode 105, then in the case of the PMOS transistor 109, the pixel output transistor 109 allows minimal current discharge, thereby preserving a high signal to be stored on the capacitor 117. If a low signal is output by the photodiode 105, then in the case of the PMOS transistor 109, the pixel output transistor 109 allows maximal current discharge, thereby preserving a low signal to be stored on the capacitor 117. In such a manner, the output of the photodiode 105 modulates the amount of charge that remains stored on the capacitor 117. The voltage that is stored on the capacitor 117 is then used to control the amplifying output transistor 119. Note that the readout result is insensitive to the precharge voltage value of the capacitor C, as long as it is consistently applied and as long as the time during the readout stage is consistent.

[0022] After the signal has been read out, the photodiode 105 is reset using the reset transistor 107. The resetting of the pixel 101 through reset transistor 107 may be done at or about the same time as the precharge operation. Note that the operation of the reset transistor 107 is commonly used to reset the photodiode 105 after the signal is read out. This process is well known in the prior active pixel art. During the reset operation, the voltage at node A is set to voltage (V_{R_reset}). As the photodiode 105 proceeds through the integration time, where the photodiode 105 is gathering light, the voltage at node A decreases in proportion to the amount of gathered light.

[0023] Several advantages of the present invention are noticed. First, because no DC current is drawn during readout, this requires less power. Indeed, calculations indicate that only approximately 10% of the power of prior readout circuits is required.

[0024] Second, there is a high uniformity and large signal range. During readout, the discharge current flows inside the readout circuit. Because there is no current on the outside power and ground lines, there is no voltage drop along the power and ground lines.

[0025] In general terms, the present invention uses a capacitor to store a predetermined charge during a precharge stage. Next, during a readout stage, the signal from a photodiode is then used to modulate the amount of charge that is discharged from the capacitor. The remaining charge on the capacitor after the discharge during the readout stage is then amplified as a signal and output.

[0026] Figure 1 illustrates one possible configuration of a readout circuit that can implement this technique. However, it can be appreciated that other configurations for the readout circuit is possible. For example, Figure 2 shows such an alternative embodiment.

[0027] In this embodiment, the capacitor 117 is charged by having the row select transistor 111 off and the precharge transistor 113 and a ground transistor S1 on. This charges the capacitor 117 to a voltage V_{DD}. After the capacitor 117 has been charged, the precharge transistor 113 and the ground transistor S1 is turned off. This allows the capacitor 117 to carry an initial voltage V_{DD}, but still allowing the capacitor 117 to discharge during a readout stage.

[0028] Specifically, during the readout stage, the row select transistor 111, the precharge transistor 113, and the transistor S0 is turned on. This allows the capacitor 117 to discharge through the pixel output transistor 109, as modulated by the signal at node A from the photodiode 105. While the term "discharge" is used, charge is actually being placed (through pixel output transistors 109, row select transistors 111, and transistor S0) onto one plate of the capacitor 117 to equalize (or "discharge") the voltage on the capacitor 117.

[0029] In some situations, it is not possible to form a discharge current path inside the readout circuit. Figure 3 shows an embodiment that remedies this situation. Specifically, Figure 3 is substantially similar to Figure 2, except that node B is not connected to node C. In this situation, during readout, there is a discharge current in the outside power and ground lines. Although the discharge current rapidly decreases rapidly with time, there is still a small voltage drop along the power and ground lines at the end of the readout stage. Thus, this embodiment is less desirable than the circuits of Figures 1 and 2, but still more desirable than the prior art.

[0030] In all of these embodiments, the capacitors in the readout circuits can be charged simultaneously or individually. For simultaneous charging, this will cause a relatively large current and associated drop in the power line. Therefore, it would be undesirable to read out data at this time.

[0031] Figure 4 shows yet another alternative embodiment. In this embodiment, the capacitor is discharged first, and then a readout step is performed. While much of the individual components are similar to that of Figures 1-3, the arrangement and operation is different. Specifically, the photodiode 105, the reset transistor 107, the pixel output transistor 109, and the row select transistor 111 are substantially configured the same as previous embodiments. However, in a first discharge stage, the row select transistor 111 is turned off and a discharge transistor 121 and hold transistor 115 is turned on. This will discharge the capacitor 117, resulting in no voltage differential between the anode and cathode (both at the same potential V_{DD}). After the discharge cycle is complete, the discharge transistor 121 and hold transistor 115 are turned off.

[0032] During the readout stage, the row select transistor 111 and hold transistor 115 is turned on. This results in the capacitor being charged by having current flow through the hold transistor 115, the row select transistor 111, and the pixel output transistor 109 to ground. In other words, the voltage at the capacitor plate connected to the gate of the amplifying output transistor 119 steadily decreases from V_{DD} towards ground as current flows. This "charges" the capacitor 117.

[0033] The amount of current flow is modulated by the signal at node A as applied to the gate of pixel output transistor 109. Thus, the amount of voltage differential between the anode and cathode of the capacitor 117 is dependent upon the pixel output transistor 109, as modulated by the signal output from photodiode 105 at node A. This signal is thus stored in the capacitor 117, and then output through the amplifying output transistor 119.

[0034] The circuit of Figure 5 works in substantially similar manner. Specifically, in a first discharge stage, the row select transistor 111 is turned off and a discharge transistor 121 and hold transistor 115 is turned on. This will discharge the capacitor 117, resulting in no voltage differential between the anode and cathode (both at the same ground potential). After the discharge cycle is complete, the discharge transistor 121 and hold transistor 115 are turned off.

[0035] During the readout stage, the row select transistor 111 and hold transistor 115 is turned on. This results in the capacitor being charged by having current flow from V_{DD} through the hold transistor 115, the row select transistor 111, and the pixel output transistor 109. In other words, the voltage at the capacitor plate connected to the gate of the amplifying output transistor 119 steadily increases from ground to V_{DD} as current flows. This "charges" the capacitor 117.

[0036] The amount of current flow is modulated by the signal at node A as applied to the gate of pixel output transistor 109. Thus, the amount of voltage differential between the anode and cathode of the capacitor 117 is dependent upon the pixel output transistor 109, as modulated by the signal output from photodiode 105 at node A. This signal is thus stored in the capacitor 117, and then output through the amplifying output transistor 119.

[0037] The embodiments of Figures 4 and 5 both generate a small current and voltage drop in the power and

ground lines at the end of the readout stage. However, the embodiments of Figures 4 and 5 can realize the discharge path inside the readout circuit easily during layout. Further, the discharge time of these embodiments is relatively short.

[0038] While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changed can be made therein without departing from the spirit and scope of the invention. For example, while the present invention has been described in terms of using a photodiode, other types of light sensing elements may also be used, such as a photogate and the like. Further, the above examples are described using a p-type substrate and photodiode. For an n-type substrate or a photogate sensor, the present invention is equally applicable to one of ordinary skill.

[0039] Thus, one of ordinary skill after reading the foregoing specification will be able to affect various changes, alterations, and substitutions of equivalents without departing from the broad concepts disclosed. It is therefore intended that the scope of the letters patent granted hereon be limited only by the definitions contained in appended claims and equivalents thereof, and not by limitations of the embodiments described herein.

Claims

1. A readout circuit comprising:

   a capacitor to be charged during a precharge stage to a predetermined voltage;
   a precharge transistor for activating during a precharge stage so as to selectively charge said capacitor to said predetermined voltage; and
   a pixel output transistor having its' gate modulated by a light signal output by a light sensing element, said pixel output transistor connected to said capacitor during a readout stage so as to selectively discharge said capacitor.

2. The readout circuit of Claim 1 further including an amplifying output transistor having its gate coupled to said capacitor such that the voltage stored on said capacitor after completion of a readout stage modulates the current flow of said amplifying output transistor.

3. The readout circuit of Claim 1 further including a row select transistor between said capacitor and said pixel output transistor.

4. A readout circuit comprising:

   a capacitor;
   a discharge transistor for activating during a discharge stage so as to selectively discharge said capacitor; and
   a pixel output transistor having its' gate modulated by a light signal output by a light sensing element, said pixel output transistor connected to said capacitor during a read out stage so as to selectively charge said capacitor.

5. The readout circuit of Claim 4 further including an amplifying output transistor having its gate coupled to said capacitor such that the voltage stored on said capacitor after completion of said read out stage modulates the current flow of said amplifying output transistor.

6. The readout circuit of Claim 4 further including a row select transistor between said capacitor and said pixel output transistor.

7. A method of reading out a light signal from a pixel comprising:

   charging a capacitor during a precharge stage;
   discharging said capacitor through a pixel output transistor, said pixel output transistor being modulated by said light signal; and
   determining the voltage held by said capacitor as an output signal.

8. The method of Claim 7 further including amplifying said output signal by placing said output signal onto the gate of an amplifying output transistor.

9. The method of Claim 7 wherein said charging of said capacitor charges said capacitor to a predetermined voltage.

10. The method of Claim 7 wherein said discharging of said capacitor is for a predetermined length of time.

11. The method of Claim 9 wherein said light signal modulates said pixel output transistor by applying said light signal to the gate of said pixel output transistor.

12. A method of reading out a light signal from a pixel comprising:

   charging a capacitor to a predetermined voltage during a precharge stage;
   discharging said capacitor for a predetermined length of time through a pixel output transistor, said pixel output transistor being modulated by said light signal by applying said light signal to the gate of said pixel output transistor; and
   determining the voltage held by said capacitor as an output signal.

13. The method of Claim 12 further including amplifying

said output signal by placing said output signal onto the gate of an amplifying output transistor.

14. A method of reading out a light signal from a pixel comprising:

discharging a capacitor;
charging said capacitor for a predetermined length of time through a pixel output transistor, said pixel output transistor being modulated by said light signal by applying said light signal to the gate of said pixel output transistor; and
determining the voltage held by said capacitor as an output signal.

15. The method of Claim 14 further including amplifying said output signal by placing said output signal onto the gate of an amplifying output transistor.

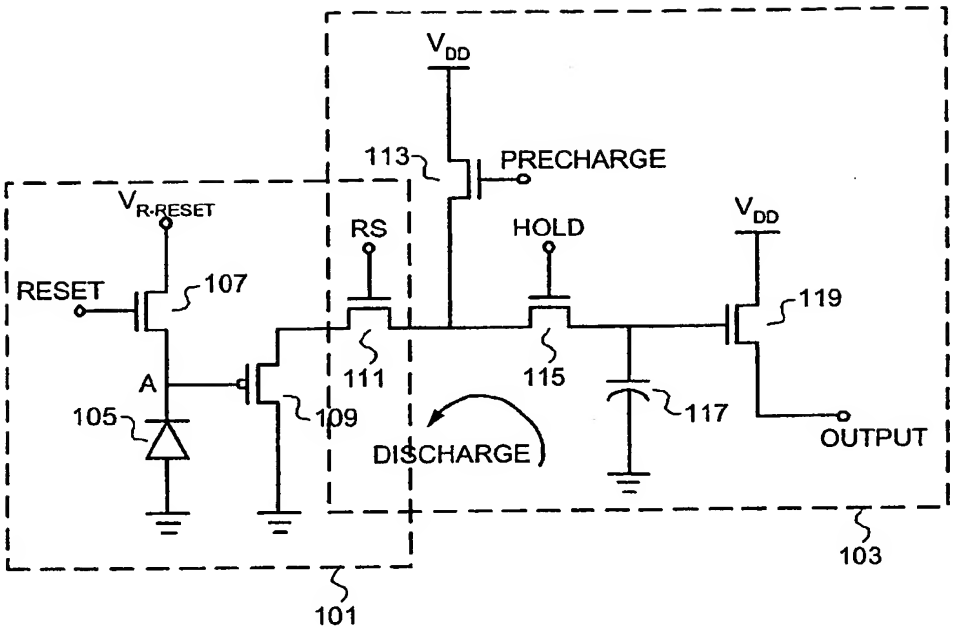
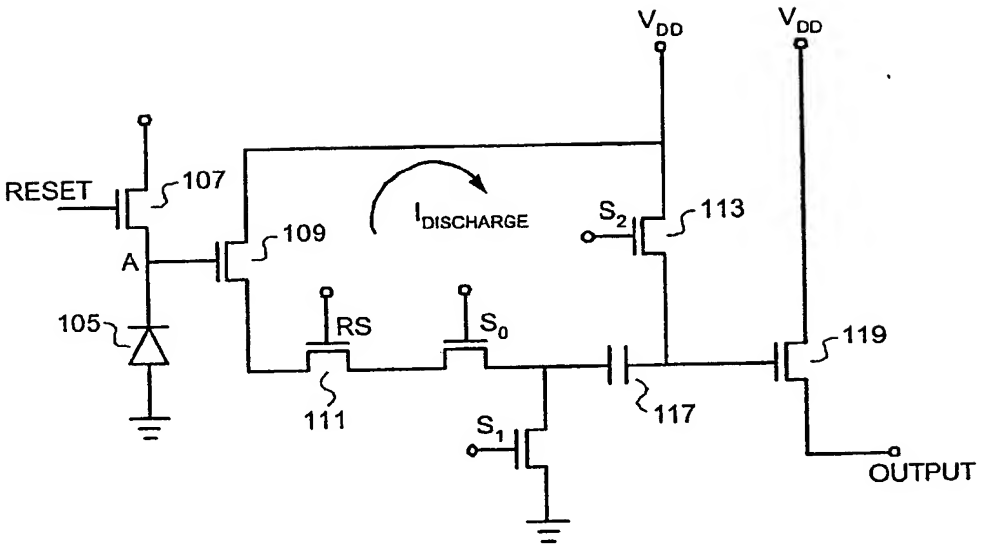

V_{DD}
113
PRECHARGE
$V_{R\text{-}RESET}$
RS
HOLD
V_{DD}
RESET
107
119
A
111
115
105
109
117
DISCHARGE
OUTPUT
103
101

FIGURE 1


V_{DD}
V_{DD}
RESET
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109
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S_2
113
A
105
RS
S_0
119
111
117
S_1
OUTPUT

FIGURE 2

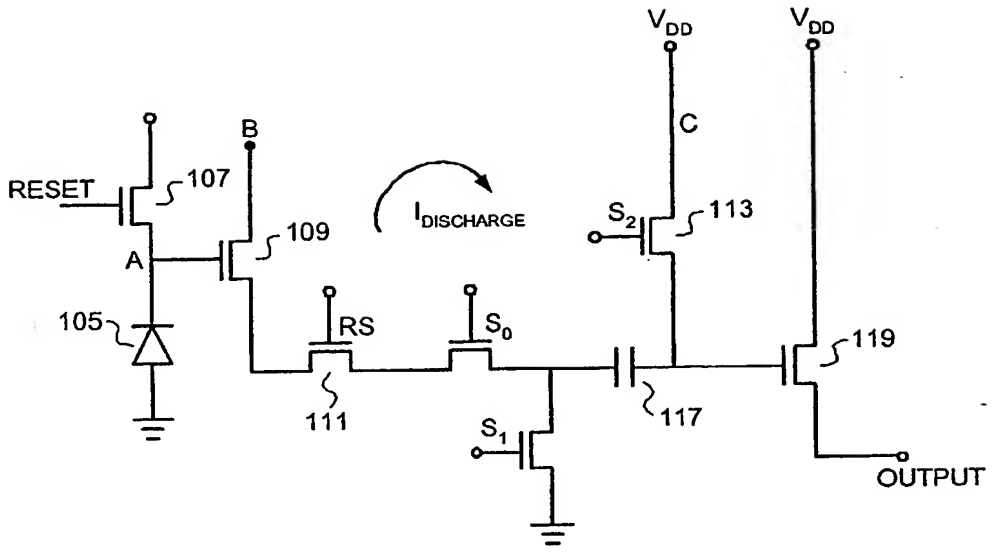
V_{DD}
V_{DD}
C
B
RESET
107
109
$I_{DISCHARGE}$
S_2
113
A
105
RS
S_0
119
111
117
S_1
OUTPUT

FIGURE 3

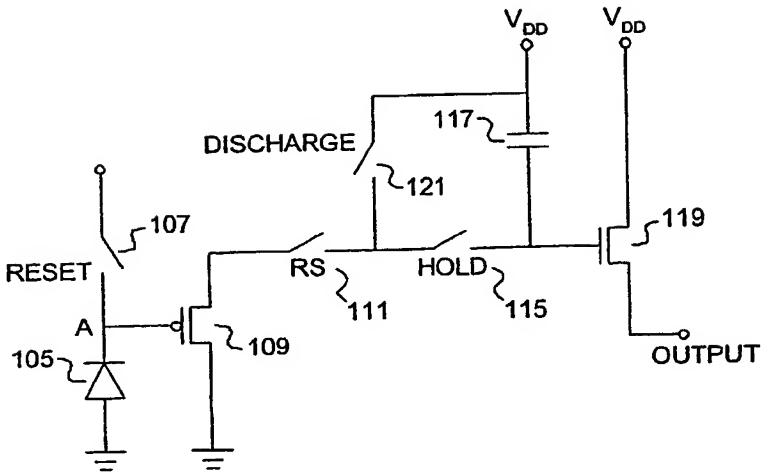

FIGURE 4

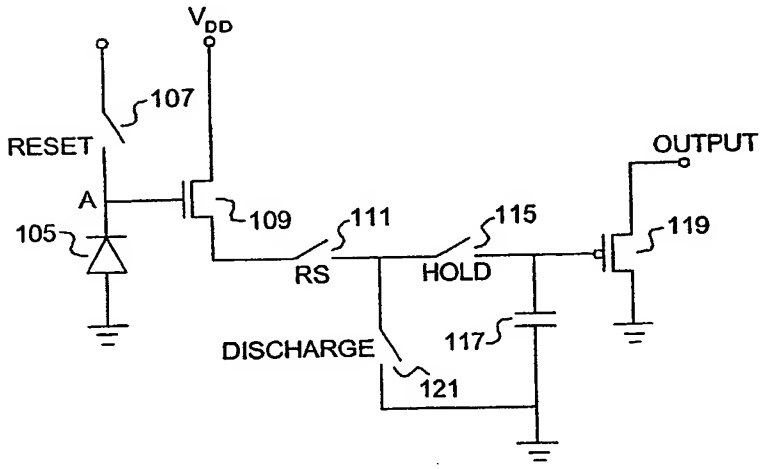

FIGURE 5

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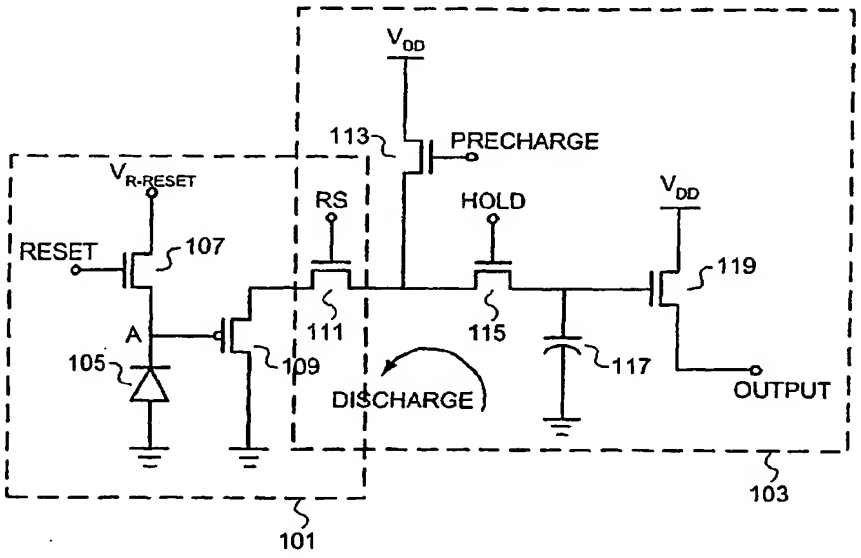

FIGURE 1

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EUROPEAN SEARCH REPORT

Application Number
EP 02 25 7636

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 969 758 A (LEVINE PETER ALAN ET AL) 19 October 1999 (1999-10-19) * column 6, line 64 - line 67; figure 1 *	1,4,7, 12,14	H04N3/15

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 November 2003	Bequet, T

CATEGORY OF CITED DOCUMENTS

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